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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/270,256	03/15/1999	ILYA KLEBANOV	0100.9900440	2265

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VEDDER PRICE KAUFMAN & KAMMHOLZ
222 N. LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
YANG, RYAN R	

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2672	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

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Office Action Summary	Application No. 09/270,256	Applicant(s) KLEBANOV, ILYA
	Examiner Ryan R Yang	Art Unit 2672

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _09 December 2002_ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _2-11,13,14,17-19,21 and 22_ is/are pending in the application.

4a) Of the above claim(s) ______ is/are withdrawn from consideration.

5)☐ Claim(s) ______ is/are allowed.

6)☒ Claim(s) _2-11,13,14,17-19,21 and 22_ is/are rejected.

7)☐ Claim(s) ______ is/are objected to.

8)☐ Claim(s) ______ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on ______ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on ______ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. ______ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ______ .
4) ☐ Interview Summary (PTO-413) Paper No(s). ______ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 12/9/02 for Continued Examination (RCE) under 37 CFR 1.53(d) based on parent Application No. 09/270,256 is acceptable and a RCE has been established. An action on the RCE follows.

2. This action is responsive to communications: Amendment, filed on 12/9/2002. This action is non-final.

3. Claims 2-11, 13, 14, 17-19, 21 and 22 are pending in this application. Claims 14, 21 and 22 are independent claims. In the Amendment, filed on 12/9/2002, claims 2, 3, 8-11, 13, 14 and 17-19 were amended, claims 1, 12, 15, 16 and 20 were canceled, and claims 21 and 22 were added.

4. The present title of the invention is "Method and Apparatus for Rendering an Image in a Video Graphics Adapter" as filed originally.

Claim Rejections - 35 USC § 102

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 21 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Noble et al. (5,657,046).

As per claim 21, Noble et al., hereinafter Noble, discloses a method of displaying active video on a computer system, the method comprising the steps of:

receiving at a first video graphics adapter (VGA) a first frame of active video from a video source (Figure 11 Video module #1);

rendering at least a first portion of the first frame of video at the first VGA in response to a first control signal, wherein the first control signal is a signal specifying a window location for displaying the active video (Figure 12 Display Control to the Display Memory Section 71); and

rendering at least a second portion of the first frame of video at a second VGA in response to a second control signal (Figure 12 channel A or channel B where the picture is scrolled; Figure 16 where second portion of the first picture is rendered in second module).

7. As per claim 14, Noble discloses a processing system for executing instructions, the processor system comprising instructions for:

monitoring the location of an active video window (Performed by the row and column counters "By manipulating the column start and stop address counters during an active display period, a complete image which is stored and centered within the video RAM matrix will shift its position to the left or right relative to the monitor screen", column 4, line 55-59);

storing active video data at first video memory (Video Module #1); and

sending the active video data from the first memory to a second memory when the location of the active video window is associated with the second video memory (Figure 10 and Figure 15-17 where the shift of video memory results in corresponding shift is display).

8. Claims 21 and 2-11 are rejected under 35 U.S.C. 102(b) as being anticipated over Kehlet et al. (5,956,046).

As per claim 21, Kehlet et al., hereinafter Kehlet, discloses a method of displaying active video on a computer system, the method comprising the steps of:

receiving at a first video graphics adapter (VGA) a first frame of active video from a video source (Figure 2 40A where the Graphics Accelerator is the VGA);

rendering at least a first portion of the first frame of video at the first VGA in response to a first control signal, wherein the first control signal is a signal specifying a window location for displaying the active video ("A digital-to-analog converter (DAC) then converts this pixel information to an analog video signals to be conveyed to a respective display device 20 via one of video cables 30", column 4, line 46-49 and "DAC unit 230 provides a select signal 224 to multiplexer 220 to select which pixel data is conveyed to DAC unit 230", column 5, line 53-55); and

rendering at least a second portion of the first frame of video at a second VGA in response to a second control signal (Figure 3 228 the Scene Switch Input Bus provides the signal to switch video).

9. As per claim 2, Kehlet demonstrated all the elements as applied to the rejection of independent claim 21, supra, and further discloses the first portion and the second portion are the same portion (since the video data is switched from the first display device to the second device, the first portion and the second portion are the same portion).

10. As per claim 3, Kehlet demonstrated all the elements as applied to the rejected claim 1, supra, and further discloses the step of rendering at least a first portion of the first frame video at the first VGA includes storing the at least a first portion of the active video in a video memory associated with the first VGA (Figure 2 and Figure 3 where each display device has its own Graphics Accelerator 40A which has its own Memory 202A,B).

11. As per claim 4, Kehlet demonstrated all the elements as applied to the rejected claim 3, supra, and further discloses rendering at least a second portion of the first frame of video at the second VGA includes the substep of:

storing the at least second portion of the active video in a first video memory associated with the first VGA (Figure 3 210).

12. As per claim 5, Kehlet demonstrated all the elements as applied to the rejected claim 4, supra, and further discloses the step of reading the second portion of the active video from the first video memory and storing the at least second portion of the active video in a first video memory associated with the first VGA (Figure 3 210 where the video signal from the first memory is read and stored).

13. As per claim 6, Kehlet demonstrated all the elements as applied to the rejected claim 5, supra, and further discloses the first video memory and second video memory are accessed by a direct memory access (DMA) controller associated with the first VGA (Figure 3 228 Scene Switch Input Bus).

14. As per claim 7, Kehlet demonstrated all the elements as applied to the rejected claim 5, supra, and further discloses the first video memory and second video memory

are accessed by a direct memory access (DMA) controller associated with the second VGA (Figure 4 228 Scene Switch Input Bus).

15. As per claim 8, Kehlet demonstrated all the elements as applied to the rejected claim 21, supra, and further discloses the first VGA is a primary VGA (where Figure 3 40A is considered primary), and the second VGA is a secondary VGA (where Figure 4 41A is considered secondary).

16. As per claim 9, Kehlet demonstrated all the elements as applied to the rejected claim 21, supra, and further discloses the first VGA is a secondary VGA (where Figure 3 40A is considered secondary), and the second VGA is a primary VGA (Figure 4 41A is considered primary).

17. As per claim 10, Kehlet demonstrated all the elements as applied to the rejected claim 21, supra, and further discloses the first VGA and the second VGA are part of a video wall such that the first frame of active video is displayed across multiple displays simultaneously ("The video display system may thus perform the scene switch simultaneously for each of the plurality of the display devices", column 3, line 47-49).

18. As per claim 11, Kehlet demonstrated all the elements as applied to the rejected claim 21, supra, and further discloses the steps of:

receiving at the second VGA a second frame of active video from a second video source (Figure 3 210 the input to the Frame Buffer is from the Previous Stage which is considered a second video source); and

rendering at least a portion of the second frame of video at the first VGA (where it is rendered in the Graphics Accelerator).

Claim Rejections - 35 USC § 103

19. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

20. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kehlet et al. (5,956,046), and further in view of Lumelsky (4,949,169).

As per claim 13, Kehlet demonstrated all the elements as applied to the rejected claim 21, supra.

Kehlet discloses a system of displaying video on multiple computer displays. It is noted that Kehlet does not explicitly disclose the step of storing the window location in a preference file, however, this is known in the art as taught by Lumelsky et al., hereinafter Lumelsky. Lumelsky discloses in a video-graphics display window environment in which the window location is stored in a preference file ("Vertical Sample Initial Address Register (SYA) 94 and Horizontal Sample Initial Address Register (SXA) 96. These two registers specify the destination window location. Two loadable counters, Vertical Sampling Address Counter (SYCNT) 98 and horizontal Sampling Address Counter (SXCNT) 100 are used as pointers to the receiving node's frame buffer (SYADDR and SXADDR)", column 14, line 30-37).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Lumelsky into Kehlet because Kehlet discloses a method of displaying video data on multiple display and Lumelsky discloses

a method of tacking the window location in order to correctly display the window on different displays.

21. Claims 22 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kehlet et al. (5,956,046), and further in view of Lauer et al. (5,523,769).

As per claim 22, Kehlet discloses a method of displaying active video on a computer system, the method comprising the steps of:

receiving at a first video graphics adapter (VGA) a first frame of active video from a video source (Figure 2 40A where the Graphics Accelerator is the VGA); and

displaying at least a first portion of the first frame of video at a second VGA in response to a second control signal (Figure 228 which switch the picture from the first display to the second display).

Kehlet discloses a system of displaying video on multiple computer displays. It is noted that Kehlet does not explicitly disclose the video source is at least one of the following: a video decoder and a television signal. However, this is known in the art as taught by Lauer et al., hereinafter Lauer. Lauer discloses a multiple display system in which "each individual unit or a subgroup is arranged to have its associated module with its own integral processor and memory responsible for font and graphics rendering, image processing, video decoding, clipping and coordination with adjacent modules", column 5, line 5-10.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Lauer into Kehlet because teaches a system of displaying video on multiple computer system and Lauer teaches the video

source can be a coded signal can be decoded by the decoding module in order to be able to decoding coded signals.

22. As per claim 17, Kehlet and Lauer demonstrated all the elements as applied to the rejection of independent claim 22, supra.

As for the video decoder is for decoding a compressed video signal, it is inherent that a video signal to be decoded is a compressed signal.

23. As per claim 18, Kehlet and Lauer demonstrated all the elements as applied to the rejection of independent claim 22, supra, and Kehlet further discloses the video source sending the first frame of data over a bus local to the first VGA (Figure 3 input to Frame Buffer Unit 210 is from Previous Stages in Graphics Pipeline).

24. As per claim 19, Kehlet and Lauer demonstrated all the elements as applied to the rejection of independent claim 22, supra, and Kehlet further discloses storing the first frame of active video in a video memory associated with the first VGA (Figure 3 since each VGA has its own corresponding frame buffer).

Response to Arguments

25. Applicant's arguments with respect to claims 21, 22 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Inquiries

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Ryan Yang** whose telephone number is **(703) 308-6133**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Michael Razavi**, can be reached at **(703) 305-4713**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Ryan Yang
January 20, 2003

MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600